The goal of this design is to implement an abstract loop as a circuit that will be space efficient for FPGA synthesis. This implements a standard while loop in which the loop test is performed before the body. To implement a do-while loop, the body unit must be placed before the storage unit.

- The pulse-generator is used to start the loop when desired.
- The mux is used to select the input data set or the result of an iteration from the body unit.
- The storage unit is an abstract interface for storing variables during the loop. This can be implemented with registers, block rams, or any other form of storage available to the thread.
- The body unit is an interface that can contain any valid circuit that obeys the go-done interface. This is designed so that the body of a loop can take more than one clock-cycle. The body unit will assert a done signal when a particular iteration is complete. It allows for arbitrarily complex designs to be implemented within the loop. For example, the body unit could be another loop.
- The loop test is a combinational circuit that asserts a signal when the loop condition fails.
- The storage controller is used to tell the storage unit when values are ready to be loaded. The storage controller takes into account the initialization pulse, system resets, the loop test, and the body unit's done signal.
- Done check is a combinational circuit that asserts done when the execution of the loop is complete.